In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1-9. Canceled

10. (New) A central base bipolar transistor made according to a method for fabricating an integrated circuit including complementary MOS transistors and an NPN-type bipolar transistor, comprising the steps of:

forming an N-type epitaxial layer on a P-type substrate, a buried layer being provided at least at a location of the bipolar transistor,

forming a thick oxide layer at locations other than locations of wells of the MOS transistors, of a collector well region of the bipolar transistor and of a base-emitter region of the bipolar transistor,

forming the wells of the MOS transistors and the collector well of the bipolar transistor,

forming the insulated gates, the spacers and sources and drains of the MOS transistors,

covering the entire structure with a protection layer including a first layer of silicon oxide and a first layer of silicon nitride,

opening the protection layer at the base-emitter location of the bipolar transistor,

forming a first P-type doped layer of polysilicon or amorphous silicon and a second layer of encapsulation oxide,

opening these last two layers at a center of the emitter-base region of the bipolar transistor,

diffusing the doping contained in the first silicon layer into the underlying epitaxial layer, to form the extrinsic base of the bipolar transistor,

implanting an N-type collector doping,

implanting a P-type doping to form an intrinsic base of the bipolar transistor,

depositing a second silicon nitride layer, depositing a second layer of polysilicon, anisotropically etching the second polysilicon layer to leave in place spacers in the vertical portions thereof, and removing the silicon nitride,

depositing a third N-type doped polysilicon layer and diffusing the doping to form the emitter of the bipolar transistor,

clearing the areas to be silicided,

performing a silicidation,

depositing a planarized insulating layer, and

performing the metallizations;

wherein the opening of the first silicon layer and of the second encapsulation layers performed so as to leave in place a central area of these layers.

11. (New) A method according to claim 10, wherein the first layer of silicon oxide has a thickness of around 20 nm and the first silicon nitride layer has a thickness of around 30 nm.

12. (New) A method according to claim 10, wherein the first silicon layer has a thickness of around 200 nm and the second silicon oxide layer has a thickness of around 300 nm.

13. (New) A method according to claim 10, wherein the first silicon layer is obtained by deposition of undoped amorphous silicon, and then by superficial implant of BF_2.

14. (New) A method according to claim 10, wherein a surface area of the collector well is doped at a same time as the sources and drains of the N-channel MOS transistors.

15. (New) A method according to claim 10, wherein the opening of the protection layer at the emitter-base location is of smaller extent than the corresponding opening in the thick oxide.

16. (New) A lateral PNP transistor made according to a method for fabricating an integrated circuit including complementary MOS transistors and an NPN-type bipolar transistor, comprising the steps of:

forming an N-type epitaxial layer on a P-type substrate, a buried layer being provided at least at a location of the bipolar transistor,

forming a thick oxide layer at locations other than locations of wells of the MOS transistors, of a collector well region of the bipolar transistor and of a base-emitter region of the bipolar transistor,

forming the wells of the MOS transistors and the collector well of the bipolar transistor,

forming the insulated gates, the spacers and sources and drains of the MOS transistors,

covering the entire structure with a protection layer including a first layer of silicon oxide and a first layer of silicon nitride,

opening the protection layer at the base-emitter location of the bipolar transistor,

forming a first P-type doped layer of polysilicon or amorphous silicon and a second layer of encapsulation oxide,

opening these last two layers at a center of the emitter-base region of the bipolar transistor,

diffusing the doping contained in the first silicon layer into the underlying epitaxial layer, to form the extrinsic base of the bipolar transistor,

implanting an N-type collector doping,

implanting a P-type doping to form an intrinsic base of the bipolar transistor,

depositing a second silicon nitride layer, depositing a second layer of polysilicon, anisotropically etching the second polysilicon layer to leave in place spacers in the vertical portions thereof, and removing the silicon nitride,

depositing a third N-type doped polysilicon layer and diffusing the doping to form the emitter of the bipolar transistor,

clearing the areas to be silicided,

performing a silicidation,

depositing a planarized insulating layer, and

performing the metallizations;

wherein:

the base region corresponds to the epitaxial layer formed above a buried layer of type N^+,

the emitter region is formed by the same implant as the sources and drains of the P-channel MOS transistors, and

the collector region is formed from a portion of the first polysilicon layer.

17. (New) A method according to claim 16, wherein the first layer of silicon oxide has a thickness of around 20 nm and the first silicon nitride layer has a thickness of around 30 nm.

18. (New) A method according to claim 16, wherein the first silicon layer has a thickness of around 200 nm and the second silicon oxide layer has a thickness of around 300 nm.

19. (New) A method according to claim 16, wherein the first silicon layer is obtained by deposition of undoped amorphous silicon, and then by superficial implant of BF_2.

20. (New) A method according to claim 16, wherein a surface area of the collector well is doped at a same time as the sources and drains of the N-channel MOS transistors.

21. (New) A method according to claim 16, wherein the opening of the protection layer at the emitter-base location is of smaller extent than the corresponding opening in the thick oxide.

22. (New) A MOS transistor resistant to electrostatic discharges made according to a method for fabricating an integrated circuit including complementary MOS transistors and an NPN-type bipolar transistor, comprising the steps of:

forming an N-type epitaxial layer on a P-type substrate, a buried layer being provided at least at a location of the bipolar transistor,

forming a thick oxide layer at locations other than locations of wells of the MOS transistors, of a collector well region of the bipolar transistor and of a base-emitter region of the bipolar transistor,

forming the wells of the MOS transistors and the collector well of the bipolar transistor,

forming the insulated gates, the spacers and sources and drains of the MOS transistors,

covering the entire structure with a protection layer including a first layer of silicon oxide and a first layer of silicon nitride,

opening the protection layer at the base-emitter location of the bipolar transistor,

forming a first P-type doped layer of polysilicon or amorphous silicon and a second layer of encapsulation oxide,

opening these last two layers at a center of the emitter-base region of the bipolar transistor,

diffusing the doping contained in the first silicon layer into the underlying epitaxial layer, to form the extrinsic base of the bipolar transistor,

implanting an N-type collector doping,

implanting a P-type doping to form an intrinsic base of the bipolar transistor,

depositing a second silicon nitride layer, depositing a second layer of polysilicon, anisotropically etching the second polysilicon layer to leave in place spacers in the vertical portions thereof, and removing the silicon nitride,

depositing a third N-type doped polysilicon layer and diffusing the doping to form the emitter of the bipolar transistor,

clearing the areas to be silicided,

performing a silicidation,

depositing a planarized insulating layer, and

performing the metallizations;

wherein the contact drain of the MOS transistor is recovered by a portion of the first polysilicon layer extending above a portion of the substrate and is also used to establish a diffusion continuing at the drain area.

23. (New) A method according to claim 22, wherein the first layer of silicon oxide has a thickness of around 20 nm and the first silicon nitride layer has a thickness of around 30 nm.

24. (New) A method according to claim 22, wherein the first silicon layer has a thickness of around 200 nm and the second silicon oxide layer has a thickness of around 300 nm.

25. (New) A method according to claim 22, wherein the first silicon layer is obtained by deposition of undoped amorphous silicon, and then by superficial implant of BF_2.

26. (New) A method according to claim 22, wherein a surface area of the collector well is doped at a same time as the sources and drains of the N-channel MOS transistors.

27. (New) A method according to claim 22, wherein the opening of the protection layer at the emitter-base location is of smaller extent than the corresponding opening in the thick oxide.

28. (New) A high voltage MOS transistor made according to a method for fabricating an integrated circuit including complementary MOS transistors and an NPN-type bipolar transistor, comprising the steps of:

forming an N-type epitaxial layer on a P-type substrate, a buried layer being provided at least at a location of the bipolar transistor,

forming a thick oxide layer at locations other than locations of wells of the MOS transistors, of a collector well region of the bipolar transistor and of a base-emitter region of the bipolar transistor,

forming the wells of the MOS transistors and the collector well of the bipolar transistor,

forming the insulated gates, the spacers and sources and drains of the MOS transistors,

covering the entire structure with a protection layer including a first layer of silicon oxide and a first layer of silicon nitride,

opening the protection layer at the base-emitter location of the bipolar transistor,

forming a first P-type doped layer of polysilicon or amorphous silicon and a second layer of encapsulation oxide,

opening these last two layers at a center of the emitter-base region of the bipolar transistor,

diffusing the doping contained in the first silicon layer into the underlying epitaxial layer, to form the extrinsic base of the bipolar transistor,

implanting an N-type collector doping,

implanting a P-type doping to form an intrinsic base of the bipolar transistor,

depositing a second silicon nitride layer, depositing a second layer of polysilicon, anisotropically etching the second polysilicon layer to leave in place spacers in the vertical portions thereof, and removing the silicon nitride,

depositing a third N-type doped polysilicon layer and diffusing the doping to form the emitter of the bipolar transistor,

clearing the areas to be silicided,

performing a silicidation,

depositing a planarized insulating layer, and

performing the metallizations;

wherein:

the high voltage MOS transistor is formed in an insulated P well;

the gate insulating layer of the high voltage MOS transistor corresponds to a portion of the protection layer including a first layer of silicon oxide and a first layer of silicon nitride;

the gate of the high voltage MOS transistor is formed from the first layer of doped polysilicon and is coated with the second layer of encapsulation oxide, the gate being laterally framed with spacers formed by the second silicon nitride layer and the second polysilicon layer; and

the source and drain contact recovery regions of the high voltage MOS transistor are formed of areas doped by diffusion from a deposition of a portion of the third polysilicon layer.

29. (New) A method according to claim 28, wherein the first layer of silicon oxide has a thickness of around 20 nm and the first silicon nitride layer has a thickness of around 30 nm.

30. (New) A method according to claim 28, wherein the first silicon layer has a thickness of around 200 nm and the second silicon oxide layer has a thickness of around 300 nm.

31. (New) A method according to claim 28, wherein the first silicon layer is obtained by deposition of undoped amorphous silicon, and then by superficial implant of BF_2.

32. (New) A method according to claim 28, wherein a surface area of the collector well is doped at a same time as the sources and drains of the N-channel MOS transistors.

33. (New) A method according to claim 28, wherein the opening of the protection layer at the emitter-base location is of smaller extent than the corresponding opening in the thick oxide.

34. (New) An EPROM transistor made according to a method for fabricating an integrated circuit including complementary MOS transistors and an NPN-type bipolar transistor, comprising the steps of:

forming an N-type epitaxial layer on a P-type substrate, a buried layer being provided at least at a location of the bipolar transistor,

forming a thick oxide layer at locations other than locations of wells of the MOS transistors, of a collector well region of the bipolar transistor and of a base-emitter region of the bipolar transistor,

forming the wells of the MOS transistors and the collector well of the bipolar transistor,

forming the insulated gates, the spacers and sources and drains of the MOS transistors,

covering the entire structure with a protection layer including a first layer of silicon oxide and a first layer of silicon nitride,

opening the protection layer at the base-emitter location of the bipolar transistor,

forming a first P-type doped layer of polysilicon or amorphous silicon and a second layer of encapsulation oxide,

opening these last two layers at a center of the emitter-base region of the bipolar transistor,

diffusing the doping contained in the first silicon layer into the underlying epitaxial layer, to form the extrinsic base of the bipolar transistor,

implanting an N-type collector doping,

implanting a P-type doping to form an intrinsic base of the bipolar transistor,

depositing a second silicon nitride layer, depositing a second layer of polysilicon, anisotropically etching the second polysilicon layer to leave in place spacers in the vertical portions thereof, and removing the silicon nitride,

depositing a third N-type doped polysilicon layer and diffusing the doping to form the emitter of the bipolar transistor,

clearing the areas to be silicided,

performing a silicidation,

depositing a planarized insulating layer, and

performing the metallizations;

wherein:

a first gate of the EPROM transistor, the associated spacers and a source and drain of the EPROM transistors are formed at the same time as those of the MOS transistors;

an insulator between gates corresponds to a portion of the protection layer, and a second gate of the EPROM transistor corresponds to the first polysilicon layer.

35. (New) A method according to claim 34, wherein the first layer of silicon oxide has a thickness of around 20 nm and the first silicon nitride layer has a thickness of around 30 nm.

36. (New) A method according to claim 34, wherein the first silicon layer has a thickness of around 200 nm and the second silicon oxide layer has a thickness of around 300 nm.

37. (New) A method according to claim 34, wherein the first silicon layer is obtained by deposition of undoped amorphous silicon, and then by superficial implant of BF_2.

38. (New) A method according to claim 34, wherein a surface area of the collector well is doped at a same time as the sources and drains of the N-channel MOS transistors.

39. (New) A method according to claim 34, wherein the opening of the protection layer at the emitter-base location is of smaller extent than the corresponding opening in the thick oxide.